

TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

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The size of this register is one byte (8 bits). Each bit has an important role in the definition of the component. Here's a breakdown of the bit roles:

CSRC: Clock Source Select bit – this bit is meaningful only in Synchronous communication in Half-Duplex mode. It “determines” if the component is Master (transmitter) or Slave (receiver). It does not matter in the case of Full-Duplex mode.

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

TX9: 9-bit Transmit Enable bit - this bit lets select the transmitted frame size 8 or 9-bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

TXEN: Transmit Enable bit

1 = Transmit enabled
0 = Transmit disabled

SYNC: USART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

BRGH - High Baud Rate Select bit – setting this bit “determines” the transmission speed (High / Low). The setting of this bit valid only for asynchronous mode, and not used for synchronous mode:

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

TRMT - Transmit Shift Register Status bit

1 = TSR empty
0 = TSR full

TX9D - Place for a 9th bit, in the case of transmitting 9-bits.